FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11429-3E

MEMORY Mobile FCRAM™
CMOS
32 M-bit (2 M word × 16 bit)
Mobile Phone Application Specific Memory
MB82DBS02163C-70L

■ DESCRIPTION

The FUJITSU MB82DBS02163C is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 33,554,432 storages accessible in a 16-bit format. MB82DBS02163C is utilized using a FUJITSU advanced FCRAM core technology and improved integration in comparison to regular SRAM. The MB82DBS02163C adopts asynchronous page mode and synchronous burst mode for fast memory access as user configurable options.
This MB82DBS02163C is suited for mobile applications such as Cellular Handset and PDA.

*: FCRAM is a trademark of Fujitsu Limited, Japan

■ FEATURES

- Asynchronous SRAM Interface
- Fast Access Time : t_{CE} = 70 ns Max
- 8 words Page Access Capability : t_{PAA} = 20 ns Max
- Burst Read/Write Access Capability : t_{AC} = 12 ns Max
- Low Voltage Operating Condition : V_{DD} = +1.65 V to +1.95 V
- Wide Operating Temperature : T_A = -30 °C to +85 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
- Low-Power Consumption : I_{DDA1} = 30 mA Max
  I_{DDS1} = 80 µA Max
- Various Power Down mode : Sleep
  4 M-bit Partial
  8 M-bit Partial
- Shipping Form : Wafer/Chip, 71-ball plastic FBGA package

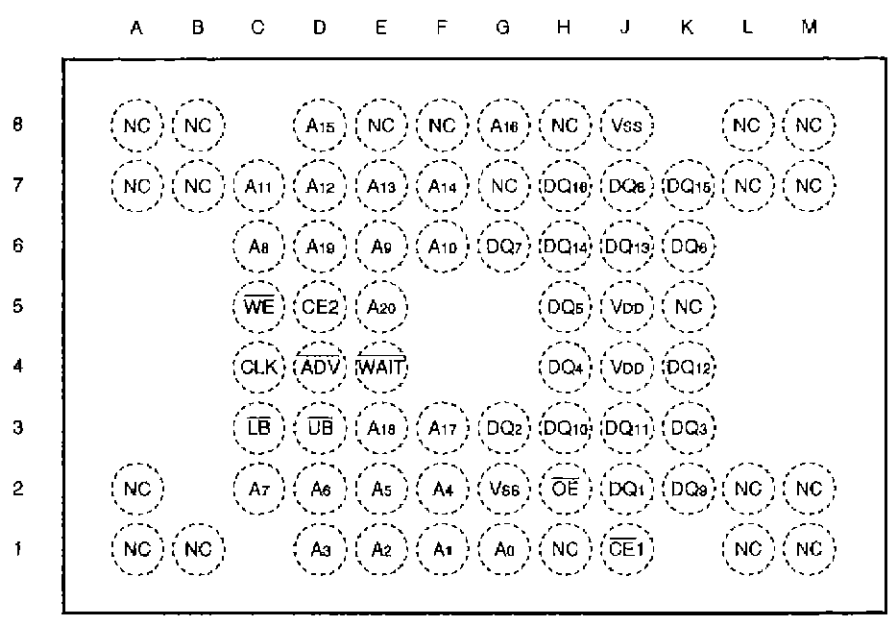
FUJITSU

■ PRODUCT LINEUP

Parameter	MB82DBS02163C-70L
Access Time (Max) (t_{CE}, t_{AA})	70 ns
CLK Access Time (Max) (t_{AC})	12 ns
Active Current (Max) (I_{DDA1})	30 mA
Standby Current (Max) (I_{DDS1})	80 µA
Power Down Current (Max) (I_{DDPS})	10 µA

■ PIN ASSIGNMENT

(TOP VIEW)

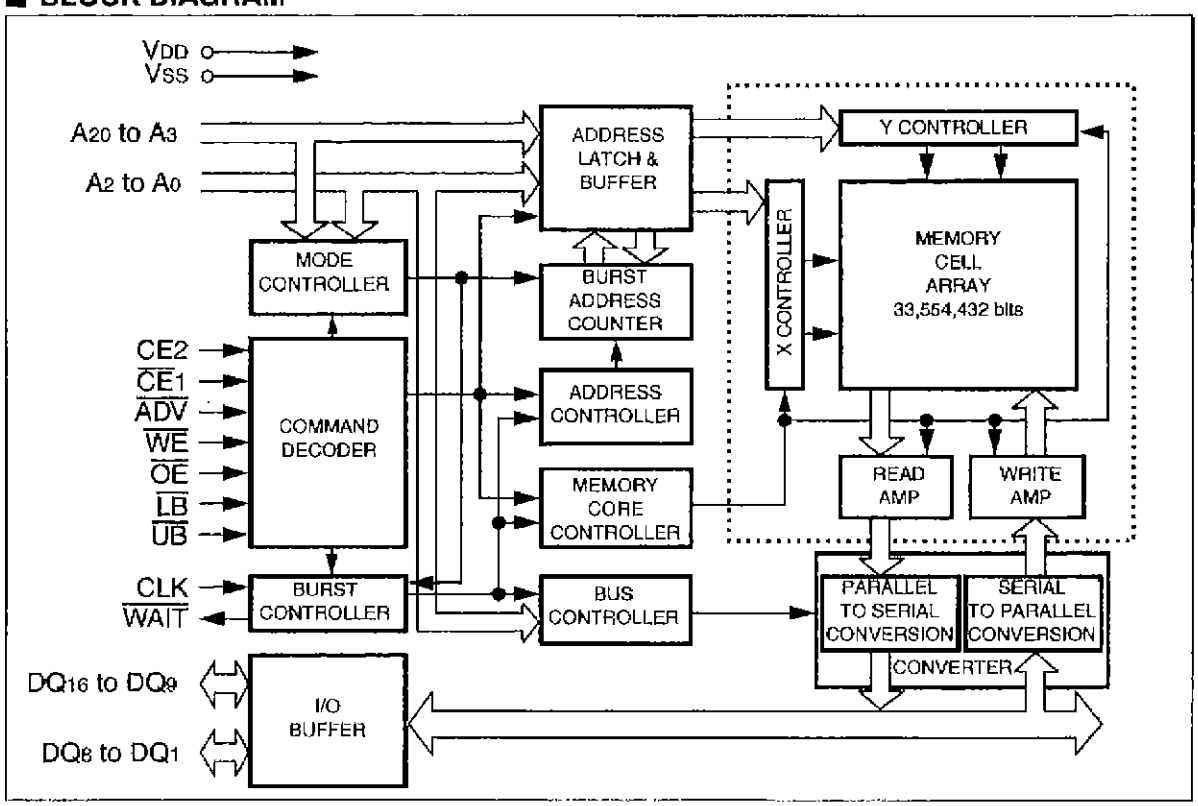


(BGA-71P-M03)

■ PIN DESCRIPTION

Pin Name	Description
A_{20} to A_0	Address Input
$\overline{CE1}$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2(High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{ADV}$	Address Valid Input (Low Active)
$\overline{WAIT}$	Wait Output
DQ_8 to DQ_1	Lower Byte Data Input/Output
DQ_{16} to DQ_9	Upper Byte Data Input/Output
V_{DD}	Power Supply Voltage
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

1. Asynchronous Operation (Page Mode)

Mode	$\overline{CE2}$	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{20} to A_0	DQ_8 to DQ_1	DQ_{16} to DQ_9	$\overline{WAIT}$
Standby (Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Output Disable*1	H	L	X	*3	H	H	X	X	*5	High-Z	High-Z	High-Z
Output Disable (No Read)			X	*3	H	L	H	H	Valid	High-Z	High-Z	High-Z
Read (Upper Byte)			X	*3	H	L	H	L	Valid	High-Z	Output Valid	High-Z
Read (Lower Byte)			X	*3	H	L	L	H	Valid	Output Valid	High-Z	High-Z
Read (Word)			X	*3	H	L	L	L	Valid	Output Valid	Output Valid	High-Z
Page Read			X	*3	H	L	L/H	L/H	Valid	*6	*6	High-Z
No Write			X	*3	L	H*4	H	H	Valid	Invalid	Invalid	High-Z
Write (Upper Byte)			X	*3	L	H*4	H	L	Valid	Invalid	Input Valid	High-Z
Write (Lower Byte)			X	*3	L	H*4	L	H	Valid	Input Valid	Invalid	High-Z
Write (Word)			X	*3	L	H*4	L	L	Valid	Input Valid	Input Valid	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1: Should not be kept this logic condition longer than 1 µs.

*2: Power Down mode can be entered from Standby state and all output are in High-Z state.
Data retention depends on the selection of Partial Size for Power Down Program.
Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3: "L" for address pass through and "H" for address latch on the rising edge of $\overline{ADV}$.

*4: $\overline{OE}$ can be V_{IL} during write operation if the following conditions are satisfied;
(1) Write pulse is initiated by $\overline{CE1}$. Refer to "(14) Asynchronous Read/Write Timing #1-1 ($\overline{CE1}$ Control)" in "■TIMING DIAGRAMS".
(2) $\overline{OE}$ stays V_{IL} during Write cycle.

*5: Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*6: Output of upper and lower byte data is either Valid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

2. Synchronous Operation (Burst Mode)

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{20} to A_0	DQ_8 to DQ_1	DQ_{16} to DQ_9	$\overline{WAIT}$
Standby(Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Start Address Latch*1	H	L	↑ *3	↓	X*4	X*4	X*6	X*6	Valid*7	High-Z*8	High-Z*8	High-Z*11
Advance Burst Read to Next Address*1	H	L	↑ *3	H	H	L	X*6	X*6	X	Output Valid*9	Output Valid*9	Output Valid
Burst Read Suspend*1	H	L	↑ *3	H	H	H	X*6	X*6	X	High-Z	High-Z	High*12
Advance Burst Write to Next Address*1	H	L	↑ *3	H	L*5	H	X*6	X*6	X	Input Valid*10	Input Valid*10	High*13
Burst Write Suspend*1	H	L	↑ *3	H	H*5	H	X*6	X*6	X	Input Invalid	Input Invalid	High*12
Terminate Burst Read	H	↑	X	H	H	X	X*6	X*6	X	High-Z	High-Z	High-Z
Terminate Burst Write	H	↑	X	H	X	H	X*6	X*6	X	High-Z	High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ↑ = valid edge, ↓ = rising edge of Low pulse, High-Z = High impedance

*1: Should not be kept this logic condition longer than 8 µs.

*2: Power Down mode can be entered from Standby state and all output are in High-Z state. Data retention depends on the selection of Partial Size for Power Down Program. Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

*3: Valid clock edge shall be set on either rising or falling edge through CR set. CLK must be started and stable prior to memory access.

*4: Can be either V_{IL} or V_{IH} except for the case the both of $\overline{OE}$ and $\overline{WE}$ are V_{IL}. It is prohibited to bring the both of $\overline{OE}$ and $\overline{WE}$ to V_{IL}.

*5: When device is operating in "$\overline{WE}$ Single Clock Pulse Control" mode, $\overline{WE}$ is Don't care once write operation is determined by $\overline{WE}$ Low Pulse at the beginning of write access together with address latching. Burst write suspend feature is not supported in "$\overline{WE}$ Single Clock Pulse Control" mode.

*6: Can be either V_{IL} or V_{IH} but must be valid before Read or Write is determined. And once $\overline{LB}$ and $\overline{UB}$ input levels are determined, they must not be changed until the end of burst.

*7: Once valid address is determined, input address must not be changed during $\overline{ADV}$ = L.

*8: If $\overline{OE}$ = L, output is either Invalid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input. If $\overline{WE}$ = L, input is Invalid. If $\overline{OE}$ = $\overline{WE}$ = H, output is High-Z.

*9: Outputs is either Valid or High-Z depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

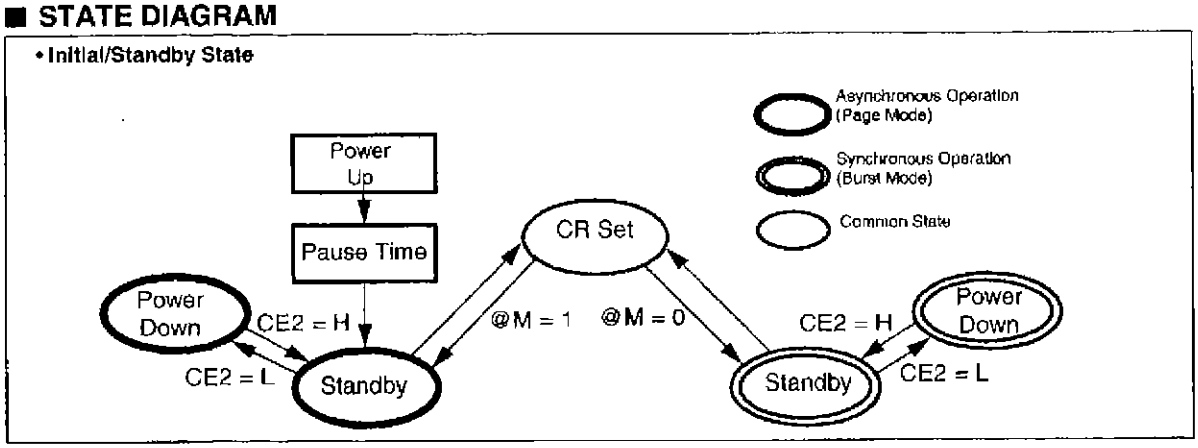
*10: Input is either Valid or Invalid depending on the level of $\overline{LB}$ and $\overline{UB}$ input.

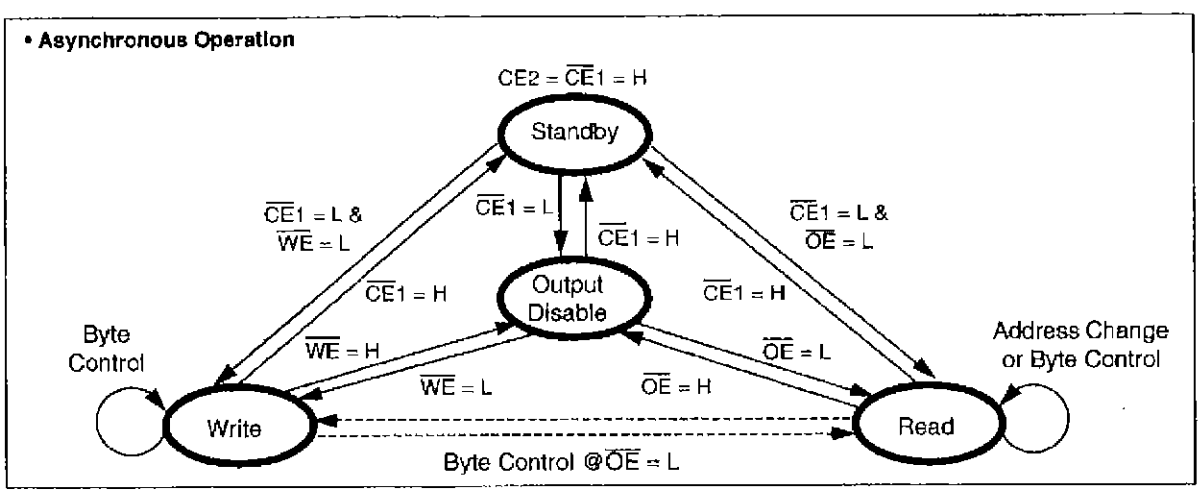
*11: Output is either High-Z or Invalid depending on the level of $\overline{OE}$ and $\overline{WE}$ input.

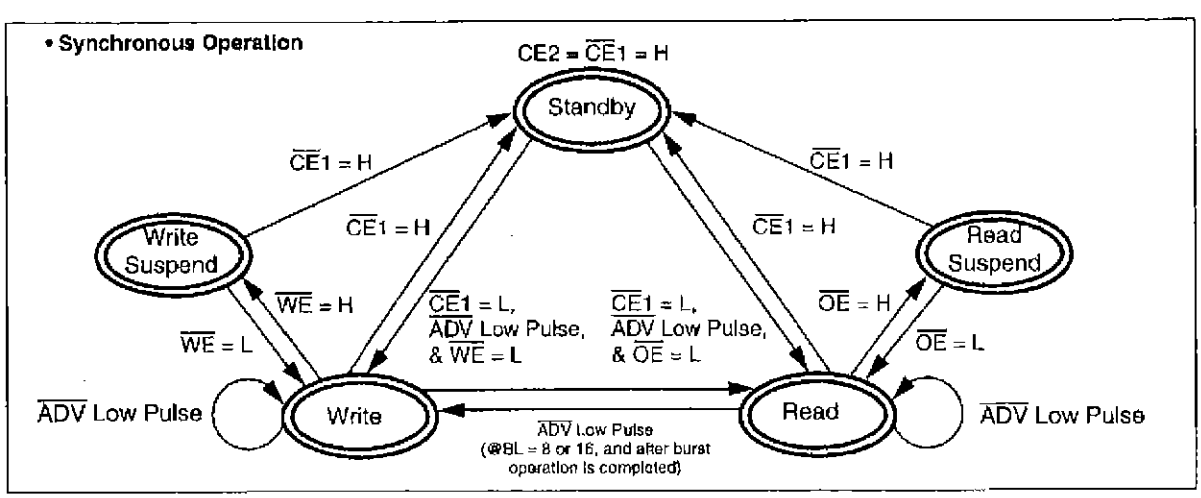
*12: Keep the level from previous cycle except for suspending on last data. Refer to "$\overline{WAIT}$ Output Function" in "■FUNCTIONAL DESCRIPTION" for the details.

*13: $\overline{WAIT}$ output is driven in High level during burst write operation.

■ STATE DIAGRAM







Note : Assuming all the parameters specified in AC CHARACTERISTICS are satisfied. Refer to the "■FUNCTIONAL DESCRIPTION", "2. AC Characteristics" in "■ELECTRICAL CHARACTERISTICS", and "■TIMING DIAGRAMS" for details.

■ FUNCTIONAL DESCRIPTION

This device supports asynchronous read, page read & normal write operation and synchronous burst read and burst write operation for faster memory access and features 3 kinds of power down modes for power saving as user configurable option.

• Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to "Power-up Timing". After Power-up, the device defaults to asynchronous page read & normal write operation mode with sleep power down feature.

• Configuration Register

The Configuration Register(CR) is used to configure the type of device function among optional features. Each selection of features is set through CR set sequence after power-up. If CR set sequence is not performed after power-up, the device is configured for asynchronous operation with sleep power down feature as default configuration.

• CR Set Sequence

The CR set requires total 6 read/write cycles with unique address. Operation other than read/write operation requires that device being in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
#1	Read	1FFFFFh (MSB)	Read Data (RDa)
#2	Write	1FFFFFh	RDa
#3	Write	1FFFFFh	RDa
#4	Write	1FFFFFh	X
#5	Write	1FFFFFh	X
#6	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address(MSB).
The second and third cycles are to write to MSB. If the second or third cycle is written into the different address, the CR set is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data(RDa) read by first cycle to MSB in order to secure the data.
The forth and fifth cycles are to write to MSB. The data of forth and fifth cycle is don't-care. If the forth or fifth cycle is written into different address, the CR set is also cancelled, but write data may not be written as normal write operation.
The last cycle is to read from specific address key for mode selection. And read data(RDb) is invalid.

Once this CR set sequence is performed from an initial CR set to the other new CR set, the written data stored in memory cell array may be lost. So, it should perform the CR set sequence prior to regular read/write operation if necessary to change from default configuration.

• **Address Key**

The address key has the following format.

Address Pin	Register Name	Function	Key	Description	Note
A_{20}, A_{19}	PS	Partial Size	00	8 M-bit Partial	
			01	4 M-bit Partial	
			10	Reserved for future use	*1
			11	Sleep [Default]	
A_{18} to A_{16}	BL	Burst Length	000	Reserved for future use	*1
			001	Reserved for future use	*1
			010	8 words	
			011	16 words	
			100	Reserved for future use	*1
			101	Reserved for future use	*1
			110	Reserved for future use	*1
			111	Continuous	
A_{15}	M	Mode	0	Synchronous Mode (Burst Read / Write)	*2
			1	Asynchronous Mode [Default] (Page Read / Normal Write)	*3
A_{14} to A_{12}	RL	Read Latency	000	Reserved for future use	*1
			001	3 clocks	
			010	4 clocks	
			011	5 clocks	
			1xx	Reserved for future use	*1
A_{11}	BS	Burst Sequence	0	Reserved for future use	*1
			1	Sequential	
A_{10}	SW	Single Write	0	Burst Read & Burst Write	
			1	Burst Read & Single Write	*4
A_9	VE	Valid Clock Edge	0	Falling Clock Edge	
			1	Rising Clock Edge	
A_8	—	—	1	Unused bits must be 1	*5
A_7	WC	Write Control	0	$\overline{WE}$ Single Clock Pulse Control without Write Suspend Function	*4
			1	$\overline{WE}$ Level Control with Write Suspend Function	
A_6 to A_0	—	—	1	Unused bits must be 1	*5

*1: It is prohibited to apply this key.

*2: If M = 0, all the registers must be set with appropriate Key input at the same time.

*3: If M = 1, PS must be set with appropriate Key input at the same time. Except for PS, all the other key inputs must be "1".

*4: Burst Read & Single Write is not supported at $\overline{WE}$ Single Clock Pulse Control.

*5: A_8 and A_6 to A_0 must be all "1" in any cases.

• **Power Down**

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

This device has 3 power down modes, Sleep, 4 M-bit Partial, and 8 M-bit Partial.

The selection of power down mode is set through CR set sequence. Each mode has following data retention features.

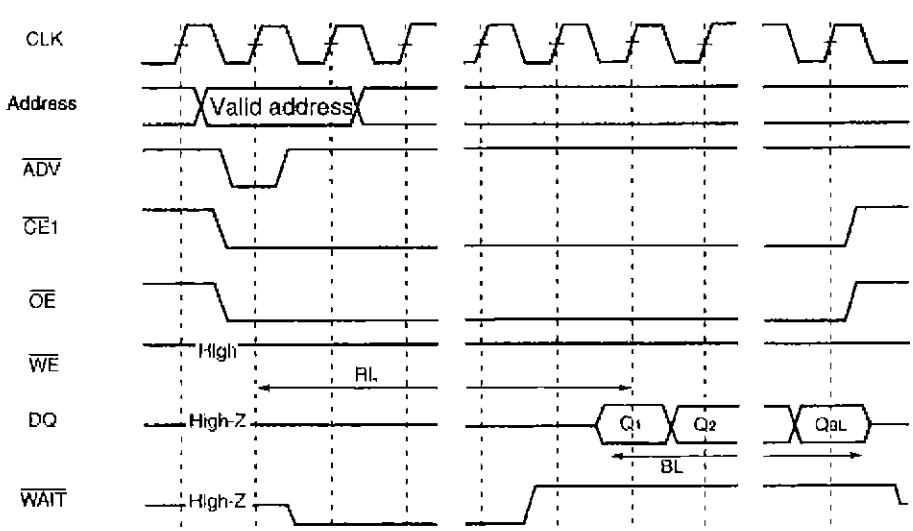
Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
4 M-bit Partial	4 M bits	000000h to 03FFFFh
8 M-bit Partial	8 M bits	000000h to 07FFFFh

The default state after power-up is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR set sequence to set to Sleep mode after power-up in case of asynchronous operation.

• **Burst Read/Write Operation**

Synchronous burst read/write operation provides faster memory access that synchronized to microcontroller or system bus frequency. Configuration Register(CR) Set is required to perform burst read & write operation after power-up. Once CR set sequence is performed to select synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR set sequence together with operation mode. In order to perform synchronous burst read & write operation, it is required to control new signals, CLK, $\overline{ADV}$ and $\overline{WAIT}$ that Low Power SRAMs do not have.

• Burst Read Operation



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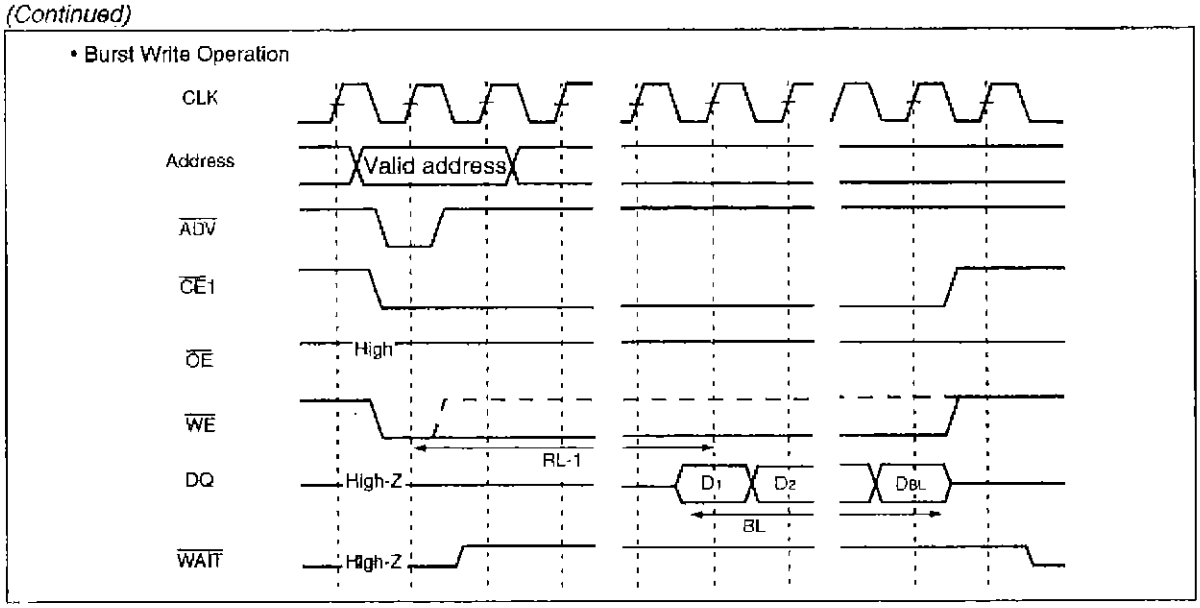


• CLK Input Function

The CLK is input signal to synchronize memory to microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and burst read data output. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is Don't care during asynchronous operation.

• $\overline{\text{ADV}}$ Input Function

The $\overline{\text{ADV}}$ is input signal to latch valid address. It is applicable to synchronous operation as well as asynchronous operation. $\overline{\text{ADV}}$ input is active during $\overline{\text{CE}}1$ = L and $\overline{\text{CE}}1$ = H disables $\overline{\text{ADV}}$ input. All addresses are determined on the rising edge of $\overline{\text{ADV}}$.

During synchronous burst read/write operation, $\overline{\text{ADV}}$ = H disables all address inputs. Once $\overline{\text{ADV}}$ is brought to High after valid address latch, it is inhibited to bring $\overline{\text{ADV}}$ Low until the end of burst or until burst operation is terminated. $\overline{\text{ADV}}$ Low pulse is mandatory for synchronous burst read/write operation mode to latch the valid address input.

During asynchronous operation, $\overline{\text{ADV}}$ = H also disables all address inputs. $\overline{\text{ADV}}$ can be tied to Low during asynchronous operation and it is not necessary to control $\overline{\text{ADV}}$ to High.

• **$\overline{\text{WAIT}}$ Output Function**

The $\overline{\text{WAIT}}$ is output signal to indicate data bus status when the device is operating in synchronous burst mode.

During burst read operation, $\overline{\text{WAIT}}$ output is enabled after specified time duration from $\overline{\text{OE}}$ = L or $\overline{\text{CE1}}$ = L whichever occurs last. $\overline{\text{WAIT}}$ output Low indicates data output at next clock cycle is invalid, and $\overline{\text{WAIT}}$ output becomes High one clock cycle prior to valid data output. During continuous burst read operation, an additional output delay may occur when a burst sequence crosses it's device-row boundary. The $\overline{\text{WAIT}}$ output notifies this delay to controller. Refer to the section "Burst Length" for the additional delay cycles in details. During $\overline{\text{OE}}$ read suspend, $\overline{\text{WAIT}}$ output does not indicate data bus status but carries the same level from previous clock cycle (kept High) except for read suspend on the final data output. If final read data output is suspended, $\overline{\text{WAIT}}$ output becomes high impedance after specified time duration from $\overline{\text{OE}}$ = H.

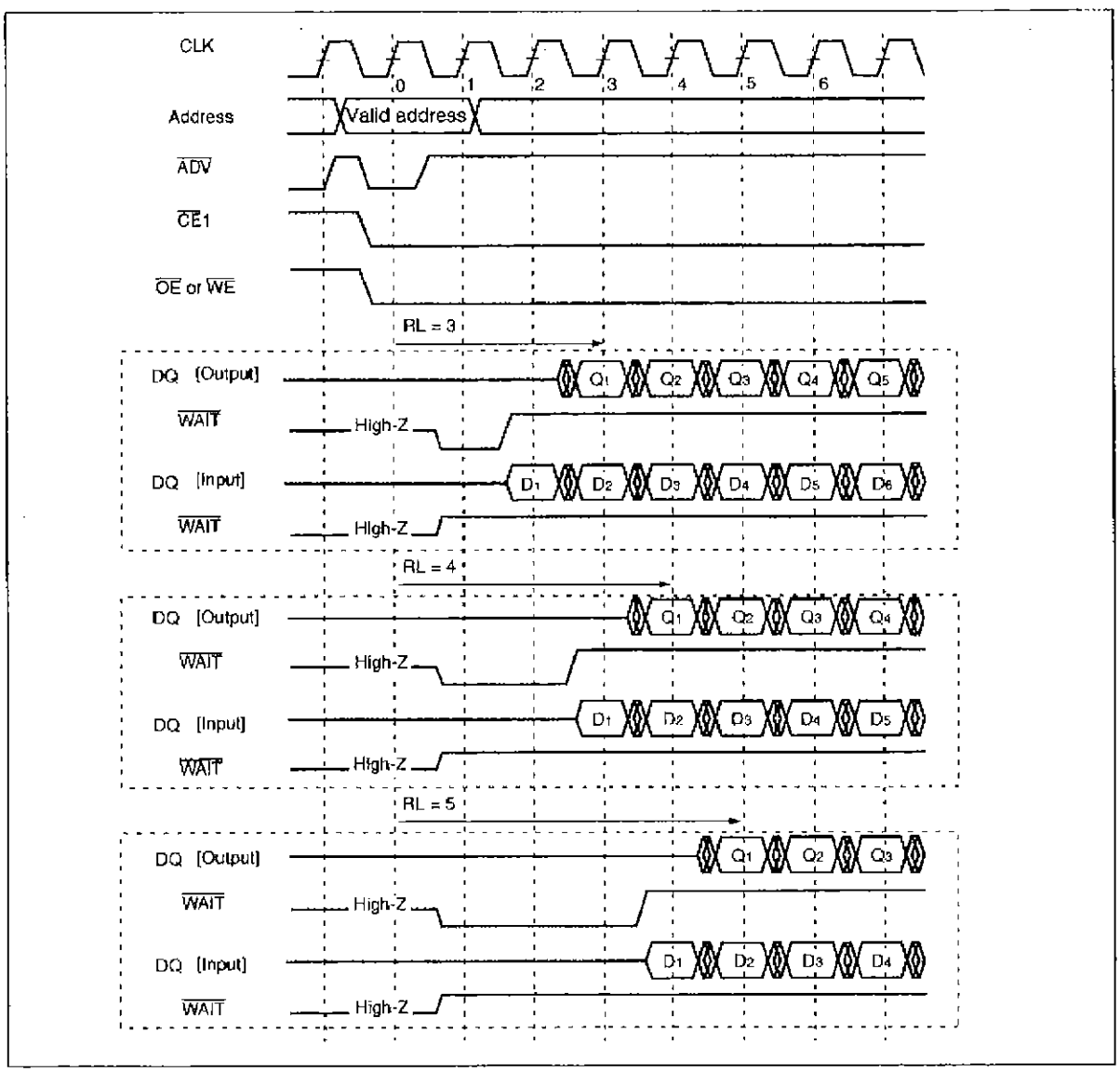
During burst write operation, $\overline{\text{WAIT}}$ output is enabled to High level after specified time duration from $\overline{\text{WE}}$ = L or $\overline{\text{CE1}}$ = L whichever occurs last and kept High for entire write cycles including $\overline{\text{WE}}$ write suspend. The actual write data latching starts on the appropriate clock edge with respect to Valid Clock Edge, Read Latency, and Burst Length. During $\overline{\text{WE}}$ Write suspend, $\overline{\text{WAIT}}$ output does not indicate data bus status but carries the same level from previous clock cycle (kept High) except for write suspend on the final data input. If final write data input is suspended, $\overline{\text{WAIT}}$ output becomes high impedance after specified time duration from $\overline{\text{WE}}$ = H.

The burst operation is always started after fixed latency with respect to Read Latency set in CR.

When the device is operating in asynchronous mode, $\overline{\text{WAIT}}$ output is always in High Impedance.

• **Latency**

Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR set sequence after power-up. Once specific RL is set through CR set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1. The burst operation is always started after fixed latency with respect to Read Latency set in CR.



• **Address Latch by $\overline{ADV}$**

The $\overline{ADV}$ latches valid address presence on address inputs. During synchronous burst read/write operation mode, all the address are determined on the rising edge of $\overline{ADV}$ when $\overline{CE}1$ = L. The specified minimum value of $\overline{ADV}$ = L setup time and hold time against valid edge of clock where RL count is begun must be satisfied. Valid address must be determined with specified setup time against either the falling edge of $\overline{ADV}$ or falling edge of $\overline{CE}1$ whichever comes late. And the determined valid address must not be changed during $\overline{ADV}$ = L period.

• **Burst Length**

Burst Length is the number of word to be read or written during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8,16 words boundary or continuous for entire address through CR set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from initial address being latched, device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). After completing read data output or write data latch for the set burst length, operation automatically ended except for continuous burst length. When continuous burst length is set, read/write is endless unless it is terminated by the rising edge of $\overline{CE}1$. During continuous burst read, an additional output delay may occur when a burst sequence cross it's device-row boundary. This is the case when A_0 to A_8 of starting address is either 7Dh, 7Eh, or 7Fh as shown in the following table. The $\overline{WAIT}$ signal indicates this delay.

Start Address (A_8 to A_0)	Read Address Sequence		
	BL = 8	BL = 16	Continuous
00h	00-01-02-...-06-07	00-01-02-...-0E-0F	00-01-02-03-04-...
01h	01-02-03-...-07-00	01-02-03-...-0F-00	01-02-03-04-05-...
02h	02-03-...-07-00-01	02-03-...-0F-00-01	02-03-04-05-06-...
03h	03-...-07-00-01-02	03-...-0F-00-01-02	03-04-05-06-07-...
...	...	...	...
7Ch	7C-...-7F-78-...-7B	7C-...-7F-70-...-7B	7C-7D-7E-7F-80-81-...
7Dh	7D-7E-7F-78-...-7C	7D-7E-7F-70-...-7C	7D-7E-7F-WAIT-80-81-...
7Eh	7E-7F-78-79-...-7D	7E-7F-70-71-...-7D	7E-7F-WAIT-WAIT-80-81-...
7Fh	7F-78-79-7A-...-7E	7F-70-71-72-...-7E	7F-WAIT-WAIT-WAIT-80-81

Note : Read address in Hexadecimal

• **Single Write**

Single write is synchronous write operation with Burst Length = 1. The device can be configured either to "Burst Read & Single Write" or to "Burst Read & Burst Write" through CR set sequence. Once the device is configured to "Burst Read & Single Write" mode, the burst length for synchronous write operation is always fixed 1 regardless of BL values set in CR, while burst length for read is in accordance with BL values set in CR.